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Respectfully submitted,



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Application Number	10/723,292
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First Named Inventor	Nikolaus Brls
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Examiner Name	Unknown
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	C1	G.D. FORNEY, JR., "The Viterbi Algorithm"; Proc. IEEE, Vol. 61, No. 3, March 1973, pp. 268-278.	
	C2	PETER J. BLACK et al. "A 140-Mb/s, 32-state, Radix-4 Viterbi Decoder"; IEEE Journal OF Solid-State Circuits, Vol. 27, No. 12, December 1992, pp. 1877-1885.	
	C3	GERHARD FETTWEIS et al. "A 100 Mbit/s Viterbi Decoder Chip: Novel Architecture and its Realization"; Proc. IEEE ICC, Vol. 2, Atlanta August 1990, pp. 463-467.	
	C4	ALFRED K. YEUNG et al. "A 210Mb/s Radix-4 Bit-level Pipelined Viterbi Decoder", 1995 IEEE International Solid-State Circuits Conference, pp. 88-89, 304.	
	C5	V.S. GIERENZ et al. "A 550 Mb/s Radix-4 Bit-Level Pipelined 16-State 0.25-µm CMOS Viterbi Decoder"; Proc. IEEE Inter.Conf. on Application-Specific Systems, Architectures, and Processors; Boston, July 2001, pp. 195-201.	
	C6	R. H. KRAMBECK et al. "High-Speed Compact Circuits with CMOS"; IEEE Journal OF Solid-State Circuits, Vol.SC-17, No. 3, June 1982, pp. 614-619.	
	C7	German Patent Office Decision to Grant dated September 30, 2003.	
	C8		

Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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